IN THE DRAWINGS

Please replace the drawings with the attached amended drawing sheets.

REMARKS

Claims 1-10 are pending in this application with claims 1-10 being amended by this response.

Objection to Drawings

The Drawings are objected to for failing to provide descriptive labels. The Drawings have been amended in accordance with the comments of the Examiner to provide proper descriptive labels. Support for the amendments to the drawings are found throughout the specification. It is respectfully submitted that no new matter is added by these amendments. In view of the amendments to the Drawings, it is respectfully submitted that this objection is satisfied and should be withdrawn.

Objection to Abstract

The Abstract is objected to for failing to comply with proper language and format. The Abstract has been amended in accordance with the comments of the Examiner to conform with the proper language and format. In view of the amendments to the Abstract, it is respectfully submitted that this objection is satisfied and should be withdrawn.

Objection to Specification

The Specification is objected to for certain informalities. The paragraph beginning on page 8, line 14, of the specification has been amended in accordance with the comments of the Examiner to provide the correct numerical reference label (53) to the subtraction stage. In view of the amendments to the specification, it is respectfully submitted that this objection is satisfied and should be withdrawn.

Objection to Claims 1-8

Claims 1-8 are objected to for certain informalities. Claims 1-8 have been amended in accordance with the comments of the Examiner to clarify the claims and provide antecedent basis for all terms. In view of the amendments to the claims, it is respectfully submitted that this objection is satisfied and should be withdrawn.

Rejection of Claims 6-8 under 35 USC § 112, First Paragraph

Claims 6-8 are rejected under 35 USC 112, first paragraph, as failing to comply with the enablement requirement.

Figures 4 and 5 have been amended to denote the block identified by reference numeral 55 as the separating stage. Support for this amendment can be found throughout the specification and specifically on page 12, line 2. It is thus respectfully submitted that no new matter is added by this amendment. The drawings now disclose that the data signal is supplied to a separating stage before rectification as claimed in claim 6. In view of the above remarks and amendments to the drawings, it is respectfully submitted that claim 6 complies with the enablement requirement of 35 USC 112, first paragraph. As claims 7 and 8 are dependent on claim 6, it is further respectfully submitted that these claims also comply with the enablement requirement of 35 USC 112, first paragraph. It is thus further respectfully submitted that this rejection is satisfied and should be withdrawn.

Rejection of Claims 1-10 under 35 USC § 112, Second Paragraph

Claims 1-10 are rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-10 have been amended in accordance with the comments of the Examiner to clarify the claims and provide antecedent basis for all terms. In view of the above remarks to the claims, it is respectfully submitted that claims 1, 4, 7, 8 and 10 comply with the enablement requirement of 35 USC 112, second paragraph. Since claims 2-3 and 5-6 are dependent on claim 1, it is further respectfully submitted that these claims also comply with the enablement requirement of 35 USC 112, first paragraph. It is thus further respectfully submitted that this rejection is satisfied and should be withdrawn.

Rejection of Claims 9 and 10 under 35 USC § 101

Claims 9 and 10 are rejected under 35 USC 101 as the claim recitation of a use, without setting forth any steps involved in the process, results in an improper definition process.

Claims 9 and 10 have been amended in accordance with the comments of the Examiner to be in the form of an apparatus claim and this comply with the requirements of 35 USC 101. In view of the amendments to claims 9 and 10, it is respectfully submitted that this rejection is satisfied and should be withdrawn.

Rejection of Claims 1-5 and 9-10 under 35 USC § 102 (b)

Claims 1-5 and 9-10 are rejected under 35 USC 102(b) as being anticipated by Tanaka (U.S. Patent No. 5,452,326).

The present claimed invention recites a phase detector for a phase-locked loop for digital input signals in which the digital summed value for a particular number of bits is equivalent to Zero. The phase detector is supplied with a sampled and digitized data signal and a delay stage for delaying the data signal by one or more sampling clock periods. The phase detector further comprises a subtraction stage to which the

undelayed and the delayed data signals are supplied, and a filter or control stage to which the output of the subtraction stage are supplied at the output of the filter or control stage which the phase error can be tapped off of. A processing stage, located between the subtraction stage and the filter or control stage, assigns one of a plurality of possible output values to the respective differential value, wherein the full differential value range is subdivided in a number of sub-ranges corresponding to the plurality of possible values so that all differential values in one of the sub-ranges will get the same output value assigned.

Tanaka describes a digital phase locked loop (PLL) circuit with a phase detector as shown in Figure 5 of Tanaka wherein a phase of an output clock is advanced by about 360 degrees at ever master clock. When a data edge has a large input level, a phase difference is calculated and the output clock frequency becomes a frequency deviated amount. Electric power consumption can thus be reduced and an automatic gain control (ACG) function is presented in the input data. The digital PLL circuit can further be given free running control and leakage secondary PLL characteristics such that the digital PLL circuit can be enhanced efficiently.

The Office Action contends that the exclusive-OR gate 79 corresponds to the claimed subtraction stage 53 of the present claimed invention. Applicant respectfully disagrees. As shown in Figure 2 of the present claimed invention, the sign of the number calculated in the subtraction is maintained. The exclusive-OR gate of Tanaka, however, is not capable of delivering a sign. In fact, the exclusive-OR gate of Tanaka is incapable of calculating the difference between two samples. In the case where two or more bit samples are delivered to the subtraction stage, the difference between 10% and 10% is 0. In Tanaka, however, the truth table of the exclusive-OR gate would generate a result of 1, which is different from the result of the present claimed invention. Consequently, Tanaka neither discloses nor suggests "comprising a subtraction stage, to which the undelayed and delayed data signals are supplied" as in the present claimed invention.

The Office Action further contends that the filter or control stage of the present claimed invention is equivalent of phase calculation ROM 77 of Tanaka. Applicant respectfully disagrees. The present claim invention recites a filter or control stage following the subtraction stage. The output of the exclusive-OR gate 79 goes to the chip select input of ROM 77. The output of the exclusive-OR gate goes to ROM 77 and not to the priority encoder. Thus, Tanaka neither discloses nor suggests "a processing stage...which assigns one of a plurality of possible output values, the respective differential values" as in the present claimed invention.

In view of the above remarks to the claims it is respectfully submitted that there is no 35 USC 112 compliant enabling disclosure in Tanaka showing the above discussed features. Since claims 2-5 and 9-10 are dependent on claim 1, it is further respectfully submitted that these claims are also patentable over Tanaka. It is thus further respectfully submitted that this rejection is satisfied and should be withdrawn.

Having fully addressed the Examiner's rejections, it is believed that, in view of the preceding amendments and remarks, this application stands in condition for allowance. Accordingly then, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicant's attorney at the phone number below, so that a mutually convenient date and time for a telephonic interview may be scheduled.

No fee is believed due. However, if a fee is due, please charge the additional fee to Deposit Account 07-0832.

Respectfully submitted,
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CERTIFICATE OF MAILING under 37 C.F.R. §1.8

I hereby certify that this amendment is being deposited with the United States Postal Service as First Class Mail, postage prepaid, in an envelope addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on:

Date: January 10, 2005 Karen Benlamich